REMARKS

Claim 11 stands objected to for minor informalities. It is respectfully submitted that the amendment to claim 11 obviates this objection. Accordingly, it is respectfully requested that the objection to claim 11 be withdrawn.

Claims 1-9 and 11-17 stand rejected under 35 U.S.C. § 112, second paragraph. It is respectfully submitted that the amendment to the claims obviates this rejection. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 112, second paragraph be withdrawn.

Claims 1-6, 8, 9 and 15 stand rejected under 35 U.S.C. § 102 as being anticipated by Doi et al. '281 ("Doi"). Claim 1 is the sole independent claim. This rejection is respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "a third step of injecting impurity ions into an active region ... such that the impurity ions ***do not reach the lower portion of the side end of the floating gate electrode in the active region***; and a fourth step of ***thermally diffusing*** the injected impurity ions by performing heat treatment on the active region, ***such that the impurity ions reach the lower portion of the side end of the floating gate electrode in the active region***" (emphasis added). Support for the added features can be found, for example, on page 13, line 12 – page 14, line 5 as well as the exemplary embodiment shown in Figures 1B to 2A with the corresponding description on page 18, line 9 – page 20, line 13 of Applicants' specification.

In contrast, Doi is completely silent as to at least the aforementioned features now set forth in claim 1. That is, Doi fails to disclose or suggest impurity ions which are injected into the active region such that the impurity ions do not reach the lower portion of the side end of the

floating gate electrode in the active region, and after the ion injection, thermally diffusing impurity ions by heat treatment such that the impurity ions reach the lower portion of the side end of the floating gate electrode in the active region.

Instead, the object of the invention disclosed in Doi (*see* Figs. 4(a) to 4(c) and the description from col. 10, line 5 to col. 11, line 27) is to suppress damages in the gate insulator film under the floating gate electrode caused by the ion injection process when forming the source/drain diffusion layers on both sides of the floating gate electrode and the control gate electrode of the stacked structure. To reach this end, Doi discloses that a CVD insulator film is formed at least on the sides of the floating gate electrode and the control gate electrode, where the CVD insulator film has a thickness to prevent the ions from being injected into the gate insulator film. Moreover, Doi discloses tilt angles at which the ions are injected (e.g., about 25 degrees for arsenic ions (Fig. 2(c)) and about 7 degrees for phosphorus ions (Fig. 4(c)).

However, Doi fails to disclose or suggest thermal diffusion after the ion injection. In other words, the source/drain diffusion layers of Doi overlap with the floating gate electrode and the control gate electrode due to the ion injection having a tilt angle.

One object of the present invention is to eliminate a long period of heat treatment required for the impurity diffusion process while suppressing damage to tunnel insulation films caused by injection of impurity ions when forming the source diffusion layer and the drain diffusion layer, which are located at side portions of the gate structure. In this regard, a short period for the heat treatment can be essential. In order to accomplish this object, a structure of the present invention can form insulation films for ion injection adjustment at least on the side surfaces of the gate structure. These insulation films for ion injection adjustment prevent impurity ions from being injected into the tunnel insulation film, and have a film thickness which

allows impurity ions to reach the portion below the floating gate electrode by a short period of heat treatment as a result of diffused scattering of impurity ions to the semiconductor substrate.

In addition, another one of the features of the present invention resides in that the impurity ions do not reach the lower portion of the side end of the floating gate electrode right after the ions are being injected into the semiconductor substrate; and the impurity ions are thermally diffused by the heat treatment for a short period after the ions are being injected into the semiconductor substrate, so that the impurity ions reach the lower portion of the side end of the floating gate electrode.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Doi does not anticipate claim 1, nor any claim dependent thereon.

The rejection of the remaining dependent claims under 35 U.S.C. § 103 rely on Doi in the same manner, whereby the secondary references relied on do not cure the deficiencies of Doi. Further, with respect to the rejection of claim 7 under 35 U.S.C. § 103 over Doi in view of Doi et al. '907, it is respectfully submitted that the present application having U.S. Serial No. 09/987,001 ("present application") and Doi et al. '907 were, at the time the invention of the present application was made, owned by Matsushita Electric Industrial Co., Ltd.. Accordingly, pursuant to MPEP § 706.02(l)(2)(II), because Doi et al. '907 is prior art to the present application only via 102(e) and because the present application was filed after November 29, 1999, Doi et al. '907 is not prior art against the present application for § 103 purposes (*see* MPEP § 706.02(l)(1,3)).

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in the remaining dependent claims because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on all the foregoing, it is respectfully submitted that all claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102 and 103 be withdrawn.

CONCLUSION

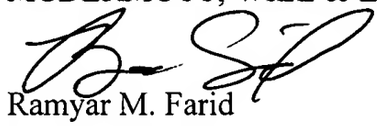
Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's

amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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